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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/955,310	09/19/2001	Sung-min Yim	SEC.813	8171

7590 06/07/2004

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EXAMINER	
PATEL, PARESH H	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 06/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	09/955,310	YIM ET AL.	
	Examiner	Art Unit	
	Paresh Patel	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2003 and 10 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *4,15-17 and 19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-14 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of Group I (claims 1-3, 5-14 and 18) in Paper filed on 03/10/2004 is acknowledged. The traversal is on the ground(s) that: 1) Group I and Group II are not related as combination/subcombination, because they are; 2) Group I and Group III are all classified in class 324 (although with slightly varying subclass), and Examiner failed to show that they are distinct; 3) no serious burden is presented to examine, because Examiner has already searched and examined all the claims of groups I, II and III.

This is not found persuasive.

First, Groups I and II are all **drawn to apparatus** that measures electrical characteristic and not as applicants noted i.e. Groups I and II are all **drawn to a method of** measuring electrical characteristic. Group III is **drawn to a method of** measuring electrical characteristic.

With respect to Groups I and II, applicants did not distinctly and specifically point what the error is. Examiner believes that claim invention of Group I and II are independent or distinct and able to support separate patents, which can also be seen from their different classification and reason provided in the last office action, see below. On page 3 of last office action Examiner stated that:

> *The combination as claimed does not require the particulars of the subcombination as claimed i.e. NMOS transistor's as claimed. The subcombination has separate utility such as control switch.*

With respect to Groups I and III, different search is required as seen from different subclass. Claim invention of Groups I and III are independent or distinct and able to support separate patents, because method of measuring electrical characteristic of Group III can be perform using any one of the apparatus as claimed in claims 1, 4 and 9 of Group I.

Because inventions are patentably distinct as mention above (also see last office action of 02/10/2004), Examiner believes that it is a serious burden to examine all the limitations of claimed different inventions. Examiner also believe that reason provided here and in the office action of 02/10/2004 are sufficient enough to provide distinctness between different inventions as claimed.

The requirement is still deemed proper and is therefore made FINAL.

Response to Arguments

Applicant's arguments response filed on 12/01/2003, with respect to claims 1-3, 5-14 and 18 of have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3 and 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kameda et al. (US 6442009) in view of Stambaugh et al. (US 4970454).

Regarding claim 1, Kameda et al. (hereafter Kameda) in fig. 3 (and at column 5) discloses an apparatus that measures electrical characteristics of an electrical element [21] within a semiconductor device [30] in a packaged state, comprising;

an electrical characteristic measurer [QN and G1] that is connected to the electrical element [2 and 21] and a pad [PAD] of the semiconductor device [30], said electrical characteristic measurer being driven in response to a control signal [TM] to output to the pad a value that is indicative of the electrical characteristics of the electrical element [lines 45-49 of column 5], the control signal being activated in an electrical characteristic measuring mode [lines 31-34 of column 5], after the semiconductor device is packaged,

wherein the pad is not connected to any output driver [see PAD in fig. 3] of the semiconductor device.

Kameda discloses all the elements except for the control signal being activated in an electrical characteristic measuring mode, after the semiconductor device is packaged. Stambaugh et al. (hereafter Stambaugh) in fig. 2 discloses the control signal being activated in an electrical characteristic measuring mode, after the semiconductor device is packaged [see abstract and lines 10-13 of column 1]. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to output a value indication of the electrical characteristics of the electrical element at pad in an electrical characteristic measuring mode as taught by Stambaugh, so various

parameters be carefully controlled to insure that the completed device (i.e. after the semiconductor device is packaged) complies with all technical specification [see lines 43-59 of column 1, particularly 43-45].

Regarding claims 3 and 8, Kameda discloses, the electrical element is selected from a group including an NMOS transistor, a PMOS transistor and a resistor [R], and the value is indicative of one of a threshold voltage and a saturation current of the NMOS transistor, one of a threshold voltage and a saturation current of the PMOS transistor, and a resistance of the resistor [lines 9-22 of column 5].

Regarding claims 5-7, Stambaugh discloses

electrical element is a transistor and selected from a group including an NMOS transistor (see Fig 7, element 96), a PMOS Transistor (see Fig 8 element 108) and a resistor (see Fig 9, element 118). Stambbaugh et al ('454) also teach that the value is Indicative of one a threshold voltage and a saturation current of NMOS transistor, one of the threshold voltage and saturation current of the PMOS transistor and a resistance of the resistor (see col. 5, lines 65-66 and col. 10, lines 67-68).

It would have been obvious to use transistor of Stambaugh as resistor R of Kameda, so electrical characteristic or process parameters of transistor can be measured.

Claims 2 and 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kameda and Stambaugh as applied to claim 1 above, and further in view of Roberts et al. (US 5734661).

Regarding claims 2, 9 and 14, Kameda and Stambaugh discloses all the elements except for control signal generator that receives at least one bit of an address signal that is received at an address pin of the semiconductor device, and that generates the control signal responsive thereto.

Roberts et al ('661) disclose an apparatus for providing external access to internal integrated circuit test circuits and expressly teach that a control signal generator (See Fig 11 element 122 below) receives **at least one bit of an address pin** (A0, n A1) of the semiconductor device and generate the control signal (TEST1, TEST2, TEST3, TEST4) responsive thereto.

It would have been obvious to one of ordinary skilled in the art at the time the invention was made to have substituted the Stambbaugh et al ('454) 's control signal generator or test mode circuit by Roberts et al ('661)'s test signal generator 122 for generating test signals in responsive to a received address signal because both references are directed to test signal generation for measuring or testing electrical elements for packaged semiconductor device, and Stambbaugh et al ('454) 's and suggested by Roberts et al ('661) (see col. 6, lines 35-36, and col. 7, lines 49-51). Therefore, the substitution of functional equivalents in Stambbaugh et al ('454) would lead to the expected success.

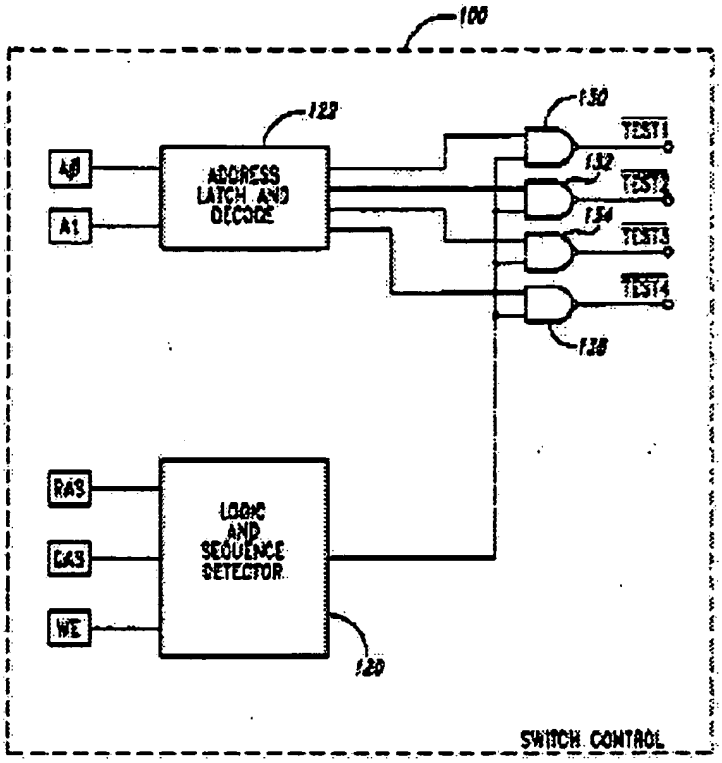

Fig. 11

Regarding claims 10 and 12, Kameda discloses, the electrical element is selected from a group including an NMOS transistor, a PMOS transistor and a resistor [R], and the value is indicative of one of a threshold voltage and a saturation current of the NMOS transistor, one of a threshold voltage and a saturation current of the PMOS transistor, and a resistance of the resistor [lines 9-22 of column 5].

Regarding claim 11, Stambaugh discloses

electrical element is a transistor and selected from a group including an NMOS transistor (see Fig 7, element 96), a PMOS Transistor (see Fig 8 element 108) and a resistor (see Fig 9, element 118). Stambbaugh et al ('454) also teach that the value is Indicative of one a threshold voltage and a saturation current of NMOS transistor, one of the threshold voltage and saturation current of the PMOS transistor and a resistance of the resistor (see col. 5, lines 65-66 and col. 10, lines 67-68).

It would have been obvious to use transistor of Stambaugh as resistor R of Kameda, so electrical characteristic or process parameters of transistor can be measured.

Regarding claim 13, Robert et al. ('661)'s address signal only has two bits (A0, A1) of the address signal.

Claim 18 rejected under 35 U.S.C. 103(a) as being unpatentable over Kameda, Stambaugh and Robert et al. ('661) as applied to claim 9 above, and further in view of Roohparvar (US 6275961).

Regarding claim 18, Kameda, Stambaugh and Robert et al. ('661) discloses all the elements except for,

Stambbaugh et al ('454) expressly teach that their electrical characteristic measurer (See Fig 7, 94) includes an NMOS transistor (98) having a drain and source, one of the drain and source being connected to the first pad (28), and the other of the drain and the source being connected to a the first pad (28) and the other of the drain and the source being connected to a terminal of the electrical element (96).

Stambbaugh et al ('454) do not show that their one of same size NMOS transistor 102 is connected to a data input/output pin.

Roohparvar ('961) disclose a method for testing an integrated memory chip (see Fig. 1) and specifically teach an NMOS transistor (M1) which is connected to a pad of a data input/output pin (30) (See Col. 4, lines 22-26).

It would have been obvious to one of ordinary skilled in the art at the time the invention was made to incorporate the teaching of Roohparvar ('961) 's NMOS transistor connected to I/O (30) into Stambbaugh et al ('454) 's electrical characteristic measurer for the purpose of allowing match between input data through the I/O pin with internal test data and thus easily and quickly identify an electrical element or a memory cell having fault as disclosed by Roohparvar ('961) (See Col. 13, lines 27-30).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paresh Patel whose telephone number is 571-272-1968. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paresh Patel
May 28, 2004